

Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action in the above-identified patent application. Claims 1-14 and 180-181 are currently pending. Claims 5-12 have been amended to correct typographical errors.

Claims 6-9 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112 and to include all of the limitations of the base claim and any intervening claims.

Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-9 are rejected as failing to define the invention in the manner required by 35 U.S.C. §112, second paragraph.

Claims 1-5 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,631,486 (*Komatsu et al.*).

I. Rejection of Claims 6-9 under 35 U.S.C. §112, Second Paragraph

Claims 6-9 are rejected as failing to define the invention in the manner required by 35 U.S.C. §112, second paragraph.

In rejecting claim 6, the Examiner stated “it is unclear which part of the semiconductor device is configured to be coupled to at least one reference signal.” Office Action, page 2.

The applicant’s attorney respectfully disagrees. Claim 6 is clear and unambiguous. The Examiner is improperly requiring the applicant to include unnecessary limitations into claim 6. The Application and Drawings disclose many embodiments of how “at least one reference signal line” may be coupled to “different parts” of “a semiconductor device.”

Claims 7-9 depend from claim 6 and therefore are patentable for at least the reasons stated above in regard to claim 6

Therefore it is respectfully requested that the rejection of claims 6-9 under 35 U.S.C. §112, second paragraph, be withdrawn.

II. Rejection of Claims 1-5 under 35 U.S.C. §102(e)

Claims 1-5 are rejected under 35 U.S.C. §102(e) as being anticipated by *Komatsu et al.*

In rejecting claim 1, the Examiner stated:

Komatsu et al. discloses in Fig. 3, a test circuit 10, a first element 31 and second element 36 wherein the first element comprises a transmitter when the second element comprises a receiver and vice versa (switch 34 can switch either first or

second element connect to either receiver 33 or transmitter 32) and second element comprising at least one transmitter and receiver 33. Office Action, page 3.

The applicant's attorney respectfully disagrees. Claim 1 calls for "A semiconductor device, comprising: a test circuit, a first element..." (Emphasis added). In contrast, Fig. 3 of *Komatsu* discloses a first semiconductor device ("DUT 30") that is a single "semiconductor integrated circuit" (Col. 8, lines 6-8) and a separate "tester 10". DUT 30 includes "first logic circuit 31" and "second logic circuit 36" along with "receiver 33" and "transmitter 32" that is separate from tester 10 that includes "data generator 11" and "comparator 12." Claim 1 of *Komatsu et al.* highlights this disclosure of two separate devices by claiming "receiving a low-transfer-rate signal from an external tester....while the integrated circuit is connected to the external tester...." (Emphasis added, Col. 11, lines 45-52.) See also claim 4 of *Komatsu et al.* that claims "an external tester." (Col. 12, line 22.)

Claims 2-5 depend from claim 1 and therefore are patentable for at least the reasons stated above in regard to claim 1.

Claims 180 and 181 are also patentable for at least similar reasons stated above in regard to claim 1.

Therefore it is respectfully requested that the rejection of claims 1-5 under 35 U.S.C. §102(e) be withdrawn.

III. Conclusion

Based on the above Amendments and these Remarks, reconsideration of claims 1-14 and 180-181 is respectfully requested.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: May 24, 2006

By: 
Kirk J. DeNiro
Reg. No. 35,854

VIERRA MAGEN MARCUS & DE NIRO LLP
575 Market Street, Suite 2500
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665